REMARKS

Claims 1-13, and 16-19 are pending in the present application. Claims 1 and 16 are independent claims, and the remaining claims are dependent claims. Claims 4, 7 and 16 have been amended, and claims 14 and 15 have been cancelled,

Claim Objections

The Examiner objected to claims 4, 7, 14, and 16 because of informalities. Claims 4, 7, 14 and 16 have been amended to correct the informalities cited by the Examiner. Accordingly, the objection to claims 4, 7, 14 and 16 is believed to have been overcome.

Claim Rejections – 35 U.S.C. § 112 ¶1

The Examiner rejected claims 14 and 15 under 35 U.S.C. § 112, paragraph 1, as failing to comply with the enablement requirement. Claims 14 and 15 have been cancelled. Accordingly, the rejection of claims 14 and 15 has been rendered moot. recites that

Claim Rejections – 35 U.S.C. § 102(e)

The Examiner rejected claims 1-13 and 16-19 under 35 U.S.C. § 102(e) as being clearly anticipated by U.S. Patent No. 6,631,452 to Lin. Applicants respectfully submit that the cited prior art reference fails to disclose each and every element of the claimed invention. Applicants submit that Lin fails to disclose, "a detector for detecting that a register window overflow condition or a register window underflow condition is imminent, by determining if execution of any fetched instructions will result in a register window overflow condition or a register underflow condition, " as recited in claim I.

Likewise, Lin fails to disclose "determining that a register window overflow condition or a register window underflow condition is **imminent** by performing a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache and determining if execution of any fetched instructions will result in a register window overflow condition or a register underflow condition, " as recited in amended claim 16. Lin discloses a register stack engine that transfers data

between frames "responsive to the available bandwidth on the memory channel," (Abstract), thus, Lin detects available bandwidth on the memory channel. As was stated in the outstanding Office Action "The system always detects that underflow/overflow is imminent..." The invention of Lin assumes that a register window overflow condition and register window underflow condition will potentially occur at some time in the future, thus it does not detect that a register window overflow condition or a register window underflow condition is **imminent** by determining if execution of any fetched instructions will result in one of a register window overflow or register window underflow. The outstanding Office Action states that the system of Lin "detects inactive procedures" and responds. Applicants respectfully submit that detecting inactive procedures is not equivalent to detecting an **imminent** spill or fill condition, as disclosed in the claimed invention of the present application. Further, the outstanding Office Action cites column 3, lines 59-67, column 4, lines 12-17, and column 4, lines 39-42, as support that Lin discloses a detector for detecting that one of the register window overflow condition and one of a register window underflow condition is imminent. These passages are directed to speculative spills and fills. As was noted in the previous paragraph, these speculative spills and fills occur in response to available bandwidth and not in response to an imminent underflow/overflow condition. Lin discloses speculative loads and stores to "increase the size of clean partition 430 at the expense of invalid partition," column 7, lines 61-62. In the same section of Lin the speculative loads are more specifically characterized in the patent as "opportunistic load operations" in column 7, lines 61 - 62. . Lin's criteria for implementing the opportunistic spill operations or fill operations are that no mandatory RSE operations are pending and that there is available bandwidth in the memory channel, column 8, lines 42-47. None of the criteria for implementation of the speculative spills and fills specify an **imminent** register window overflow condition or register window underflow condition, thus the opportunistic (speculative) operations are not responsive to that condition. Additionally, Lin fails to disclose, "an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap to avoid stalling the microprocessor," as recited in claim I, and, "in response to determining that the one of the register window overflow

condition or register window underflow condition is imminent, manipulating the storage to avoid a trap, " as recited in claim 16. When faced with an spill or fill, the register stack engine of Lin executes a mandatory register stack engine (RSE) operation, (Figure 5), "If the RSE state indicates that mandatory spill or fill operations are necessary, these are implemented and the RSE state is adjusted accordingly," (column 9, lines 1-3 and Figure 5). The mandatory RSE operation may stall the microprocessor, "Mandatory spill and fill operations may cause the processor to stall if the active procedure can not make forward progress until the mandatory spill/fill operations complete," (column 3, lines 2-5). When faced with a spill or fill Lin uses mandatory operations which may stall the processor, thus, Lin does not disclose all of the elements of claim I and claim 16. Stated differently, claims 1 and 16 recite performing an operation to prevent a spill or fill operation which is imminent whereas Lin discloses performing a conditional operation based upon available bandwidth. Since Lin discloses a **conditional** operation while claims 1 and 16 disclose performing an **unconditional** operation upon detection that a register window overflow or a register window underflow is imminent, Lin does not disclose each and every element of independent claims 1 and 16, which are therefore patentable. Claims 2-13 depend from claim1l and claims 17-19 depend from claim 16. Accordingly, claims 2-13 and 17-19 are therefore patentable as being dependent on an allowable base claim in addition to their own claimed characteristics.

Claim Rejections – 35 U.S.C. § 102(b)

The Examiner rejected claims 1, 2, 6, 8, and 11-15 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,377,336 to Eickemeyer. Claims 14 and 15 have been cancelled. Eickemeyer is generally directed to a load unit for processing the data fetch in load instructions. By processing the fetch early, cache misses can be processed in parallel with other execution thereby reducing the performance degradation of cache misses.

Applicants respectfully submit that the cited prior art reference fails to disclose each and every element of the claimed invention. Applicants submit that Eickemeyer fails to disclose "a detector for detecting an instruction in a cache prior to execution of

said instruction indicating that a trap requiring an access to the storage to manage register window information is imminent, by determining if execution of any fetched instructions will result in a register window overflow condition or a register underflow condition; " as recited in amended claim 14.

Eickemeyer does not disclose a detector as specified in claim 1. The previous Office Action cites column 3, lines 30-47 as evidence that Eickemeyer discloses such a detector. Applicants respectfully submit that a detector for load instructions (as disclosed in Eickemeyer) is not equivalent to detector for detecting that a register window overflow condition or a register window underflow condition is imminent, by determining if execution of any fetched instructions will result in a register window overflow condition or a register underflow condition In Eickemeyer, every load instruction in the instruction buffer results in a prefetch, column 7, lines 1-11. Eickemeyer does not determine if execution of any fetched instructions will result in a register window overflow condition or a register underflow condition.

Further, the detector of Eickemeyer detects load instructions in an instruction buffer, "The load unit 107 detects data fetch instructions from the I-buffer 105, predicts the address of the data to be fetched, and processes the fetch...," (column 7, lines 2-5). This is also illustrated in FIG. I where the load unit is in direct communication with the I-BUFFER (instruction buffer). A buffer is not equivalent to a cache. While both are memory, they are different in structure function and operation. A cache is a small fast memory holding recently accessed data, designed to speed up subsequent access to the same data. In contrast a buffer is an area of memory used for storing messages with an input pointer, and output pointer and a count of the space that is used or free. Replacing a cache with a buffer in a computer, or vice versa, would result in a non-functional computer, thus a buffer is not equivalent to a cache.

Further, claim 1 recites detecting that two conditions can occur (a register window underflow condition or a register window overflow condition) whereas Eickemeyer only discloses detecting a single condition (arguably a register window underflow condition). Therefore, for all the reasons above, claim 1 is allowable over

Eickmeyer. Claims 2, 6, 8, and 11-13 depend from claim 1 and are believed allowable as they depend fro a base claim which is believed allowable.

In view of the above, the Examiner's objections and rejection are believed to have been overcome, placing claims 1-13 and 16-19 in condition for allowance and reconsideration and allowance thereof is respectfully requested.

Applicants hereby petition for any extension of time required to maintain the pendency of this case. If there is any fee occasioned by this response that is not paid, please charge any deficiency to Deposit Account No. 50-3735.

Should the enclosed papers or fees be considered incomplete, Applicants respectfully request that the Patent Office contact the undersigned collect at the telephone number provided below.

Applicants invite the Examiner to contact the Applicants' undersigned Attorney if any issues are deemed to remain prior to allowance.

Respectfully submitted,

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